REMARKS

Claims 1-20 are pending. In Box 1 of the September 17, 2003 Office Action, the Examiner indicated that the Response was responsive to Communications filed on 8/30/00, 9/9/00, and 7/19/01. While Applicant indeed filed the above-referenced patent application on 8/30/00, Applicant did not file any additional Communications on or about 9/9/00 or 7/19/01. In addition, in Box 9 of said Office Action, the Examiner indicated an objection to the Specification, yet no objection was articulated in the Examiner's written Response. Consequently, Applicant seeks clarification on both of these points.

In the interest of clarity, the following Item Numbers correspond to the Examiner's Item Numbers in the Office Action:

1-2. The Examiner rejected Claims 1-3, 6, 13-16, and 18-19 under 35 U.S.C. § 102(b) as being anticipated by U.S. Pat. No. 5,907,498 ("Rim"). Respectfully, Applicant traverses and requests withdrawal.

More specifically, the Examiner asserts that Rim discloses that the determining and predicting step occurs substantially in parallel with the performing step. However, Rim, in fact, discloses that an overflow detector 150 detects an overflow condition based on three inputs—namely, "the output of a barrel shifter, the output of a code extender **and a carry signal produced by an ALU.**" *Col. 2, lines 14-16 (emphasis added). See also id. at lines 26-30* ("An overflow detector...is configured to receive the a component of the first operand, the b component of the second operand **and an (N-1)-th carry C_{N-1} signal from the arithmetic logic unit**, and responsive thereto, generate an output signal indicating whether an overflow condition is generated...") (emphasis added) *and FIG. 3*. Moreover, the Examiner acknowledged as such in his written Response: "Rim discloses in Figure 3 a most significant bit of the product (C30) connect [sic] to overflow detector..." *Detailed Action, Page 4, Item 4.* Thus, the overflow detection calculation does not truly occur in parallel with the ALU computation, but rather, the former is necessarily dependant on the latter. *See Fig. 3.* In Applicant's invention, on the other hand, the determining and predicting step indeed occurs substantially in parallel with the performing step, the former being truly independent from the latter. In other words, Applicant's, unlike Rim's, determining and predicting step occurs substantially in parallel with the performing step. Moreover, both operations occur substantially in parallel *and independently.* To clarify, Applicant accordingly amended Claims 1-3, 5-7, 13, and 15. Moreover, Applicant

also respectfully asserts that Rim, unlike Applicant, does not disclose, teach, or suggest at least *partially* performing arithmetic operations.

3-4. The Examiner rejected Claims 4-5, 7-12, 17, and 20 under 35 U.S.C. § 103(a) as being obvious over Rim in view of U.S. Pat. No. 5,508,951 ("Ishikawa") in further view of U.S. Pat. No. 5,943,249 ("Handlogten"). Respectfully, Applicant traverses and requests withdrawal.

More specifically, the Examiner correctly notes that Rim does not disclose logically ORing the simple clamp predictor with a most significant bit of the product or counting a number of leading logical zeros in positive operands, leading logical ones in negative operands, and then summing the results. *See Detailed Action, Page 4, Item 4.* In disagreement with the Examiner, however, Applicant respectfully asserts that neither Ishikawa nor Handlogten make up for these deficiencies.

Ishikawa, for example, discloses, in FIG. 2, logically ORing the "MOST SIGNIFICANT BIT IN ALU5" with "CARR FROM NEXT HIGHER-ORDER POSITION." *See FIG. 2.* However, such logical operation occurs *internally within* the Overflow Detection Circuit 6 of FIG. 1, to wit: "Referring now to the drawings...particularly to FIG. 1...[t]he overflow-detection circuit 6 is connected to the ALU 5 and includes a circuit structure, as shown in FIG. 2..." *Col. 4, line 66 – Col. 5, line 12.* In other words, FIG. 2 depicts the circuitry of the Overflow Detection Circuit 6 of FIG. 1, by which the logically ORing operation occurs *internally within* the Overflow Detection Circuit 6. In Applicant's invention, on the other hand, logically ORing the simple clamp predictor with the most significant bit of the product does not occur as an internal step within an Overflow Detection Circuit, but rather, as a subsequent step thereto. Thus, Applicant's determining and predicting step is able to occur substantially in parallel and independent from Applicant's performing step. Accordingly, Applicant respectfully asserts that the combination of Rim and Ishikawa lacks any suggestion for their combination in a manner required to meet Applicant's claims. Even if combined, however, the references do not meet Applicant's claims. And finally, contrary to the Examiner's suggested "reduce the circuitry" motivation to "improve the system performance for detecting overflow," Applicant's separate step of logically ORing the simple clamp predictor with the most significant bit of the product following ALU and Overflow Detection processing does not accomplish the latter by operation of the former. Rather, Applicant has not enhanced performance by reducing circuitry, but by

performing ALU and Overflow Detection processing substantially in parallel and independently from one another.

Handlogten, on the other hand, is directed towards floating-point calculations. *See, e.g., Title* ("Method and Apparatus to Perform Pipelined Denormalization of **Floating-Point Results**") (emphasis added), *Abstract* ("A method of processing **floating-point instruction**...in a **floating-point processor**") (emphasis added), *and Col. 1, lines 7-9* ("The present invention...relates to...a method of processing denormalized **floating-point numbers**") (emphasis added). Moreover, Applicant respectfully asserts that the Examiner may have misunderstood Handlogten, or alternatively, failed to present a convincing line of reasoning as to why Applicant's claimed subject matter would have been obvious in view thereof. More specifically, Handlogten's multiplier 212, directed toward floating-point manipulations, receives the mantissas of two operands (A and C at 202 and 206, respectively), and then reduces the arithematic function result to two separate intermediate results—called "sum" and "carry"—that are provided to a main adder/incrementer 222. *See Col. 5, lines 53-57.* Handlogten then uses a Leading Zero Anticipator ("LZA") to determine the number of zeros to remove from its intermediate results, and then a physical Leading Zero Overlay ("LZO") to shift these intermediate results by an amount corresponding to an intermediate **exponent**. *See Col. 7, lines 52-59.* In fact, according to Handlogten,

> The result is then fed to a conventional LZA which determines the number of leading zeros to remove from the intermediate result. It can thus be seen that the LZO effectively limits the LZA to shifts of the intermediate result by an amount corresponding to the intermediate exponent. In this manner, the LZA never creates an exponent less than E_{min} where E_{min} is the minimum exponent value.

Id. This appears to be a different principle of operation than Applicant's counting a number of leading logical zeros for positive operands and leading logical ones for negative operands, as described throughout the Specification and claimed in Claims 4 and 10-12. Presented in table format in Handlogten's Table 1, Handlogten's LZO "is based on the intermediate exponent stored in the intermediate register 224." *Id. at lines 18-20.* Thus, unlike in Applicant's invention, which is directed towards fixed-point numbers and not floating-point numbers, Handlogten does not disclose, teach, or suggest using LZAs and LZOs to determine numbers of logical ones and zeros in operands themselves (as opposed to exponents), nor summing logical

ones and zeros, whether individually or collectively, as described throughout the Specification and claimed in Claims 4 and 10-12.

Accordingly, Applicant respectfully asserts that the Examiner has not established a *primae facie* case of obviousness with respect to Rim in view Ishikawa in further view of Handlogten.

CONCLUSION

Applicant believes Applicant has overcome the Examiner's rejection of Claims 1-20 under 35 U.S.C. §§ 102(b) and 103(a). Moreover, Applicant believes Claims 1-20 are patentable. Thus, Applicant respectfully submits that all pending claims are in a condition for allowance, which Applicant respectfully requests.

Applicant believes this Response should allow the Examiner to allow the above-referenced patent application to issue as a U.S. patent without further amendments to the specification or claims. Thus, Applicant also requests notification to that effect.

If questions should arise, please telephone the undersigned attorney.